

## CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

*Sub. a1*  
1. A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal and said second enable signal to obtain a first sample of said DTE data signal at said first time and a second sample of said DTE data signal at said second time, and for determining whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

*01 Cont*  
2. The circuit of claim 1, wherein the frequency of said master clocking signal is approximately 8 times the frequency of said DCE clocking signal.

3. The circuit of claim 1, wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal.

1 *Sub*  
 2 *CO.* The circuit of claim 1, wherein said sample comparator generates a selector control signal if said first sample is different from said second sample.

1 5. The circuit of claim 4, further comprising:  
 2 an inverter producing an inverted circuit clocking signal from said circuit  
 3 clocking signal; and  
 4 a selector producing an output signal that is selected from the group consisting  
 5 of said circuit clocking signal and said inverted circuit clocking signal, in response to  
 6 said selector control signal.

*Sub 2*  
 1 6. A circuit for detecting errors in the synchronization of a DTE (data terminal  
 2 equipment) data signal with a DCE (data communication equipment) clocking signal, in a  
 3 communication environment wherein the DCE interfaces the DTE to a communication  
 4 channel, the circuit comprising:  
 5 means for obtaining a first sample of said DTE data signal at a first time;  
 6 means for obtaining a second sample of said DTE data signal at a second time,  
 7 said second time being subsequent to said first time, the interval between said first  
 8 time and said second time being less than the period of the DCE clocking signal; and  
 9 means for comparing said first sample to said second sample.

*DI cont*  
 1 7. The circuit of claim 6, wherein the interval between said first time and said  
 2 second time is approximately 1/8 of the period of the DCE clocking signal.

1 8. The circuit of claim 6, further comprising:  
 2 means for generating a selector control signal if said first sample is different  
 3 from said second sample.

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 1 9. The circuit of claim 8, further comprising:  
 2 means for inverting said DCE clocking signal in response to said selector  
 3 control signal.

1 10. The circuit of claim 9, further comprising:  
 2 means for transmitting said inverted DCE clocking signal from said DCE to  
 3 said DTE in lieu of said DCE clocking signal.

1 11. A method for detecting errors in the synchronization of a DTE (data terminal  
 2 equipment) data signal with a DCE (data communication equipment) clocking signal, in a  
 3 communication environment wherein the DCE interfaces the DTE to a communication  
 4 channel, the method comprising the steps of:

5 obtaining a first sample of said DTE data signal at a first time;

6 obtaining a second sample of said DTE data signal at a second time, said  
 7 second time being subsequent to said first time, the interval between said first time and  
 8 said second time being less than the period of the DCE clocking signal; and

9 comparing said first sample to said second sample.

1 12. The method of claim 11, wherein the interval between said first time and said  
 2 second time is approximately 1/8 of the period of the DCE clocking signal.

1 13. The method of claim 11, further comprising the step of:  
 2 generating a selector control signal if said first sample is different from said  
 3 second sample.

1 14. The method of claim 13, further comprising the step of:  
 2 inverting said DCE clocking signal in response to said selector control signal.

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1 15. The method of claim 14, further comprising the step of:  
 2 transmitting said inverted DCE clocking signal from said DCE to said DTE in  
 3 lieu of said DCE clocking signal.

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